WHAT IS CLAIMED IS:

- 1. A routing multiplexer system providing p outputs based on a selected permutation of p inputs, the multiplexer system comprising:
- a plurality of modules each having first and second inputs, first and second outputs and a control input and arranged to supply signals at the first and second inputs to the first and second outputs in a direct or transposed order based on a value of a bit at the control input, a first p/2 group of the modules being coupled to the n inputs and a second p/2 group of the modules being coupled to the n outputs; and
- a memory containing plurality of control bit tables each containing a plurality of bits in an arrangement based on a respective permutation, the memory being responsive to a selected permutation to supply bits to the respective modules based on respective bit values of a respective control bit table.
- 2. The multiplexer system of claim 1, wherein the modules are arranged in an array of rows, and each control bit table contains rows each containing a plurality of bits, the memory supplying a j-th bit at an i-th row of a selected control bit table to the corresponding j-th module of the i-th row of the array.

- 3. The multiplexer system of claim 2, wherein there are at least $(2k-1)\times 2^{k-1}$ modules and at least $(2k-1)\times 2^{k-1}$ bits and the array of modules and each control bit table has 2k-1 rows, where $p=2^k$ and k>0.
- 4. The multiplexer system of claim 1, wherein there are at least $(2k-1)\times 2^{k-1}$ modules and at least $(2k-1)\times 2^{k-1}$ bits, where $p=2^k$ and k>0.
- 5. An integrated circuit chip containing a circuit for mapping up to p memories for parallel turbo decoding, the circuit comprising:
 - a routing multiplexer having:
 - a plurality of modules each having first and second inputs, first and second outputs and a control input and arranged to supply signals at the first and second inputs to the first and second outputs in a direct or transposed order based on a value of a bit at the control input, and
 - a permutation memory containing plurality of control bit tables each containing a plurality of bits in an arrangement based on a respective permutation,
 - map inputs coupling an output of each memory to
 respective ones of the first and second
 inputs of a first p/2 group of the modules;

- map outputs coupled to respective ones of the first and second outputs of a second p/2 group of the modules; and
- a permutation selection device coupled to the permutation memory for operating the permutation memory to select a respective control bit table to supply bits to the control inputs of the modules.
- 6. The mapping apparatus of claim 5, wherein the modules are arranged in an array of rows each containing p/2 modules, and each control bit table contains rows each containing p/2 bits, the memory supplying a j-th bit at an i-th row of a selected control bit table to the corresponding j-th module of the i-th row of the array.
- 7. The mapping apparatus of claim 6, wherein there are at least $(2k-1)\times 2^{k-1}$ modules and at least $(2k-1)\times 2^{k-1}$ bits and the array of modules and each control bit table has 2k-1 rows, where $p=2^k$ and k>0.
- 8. The mapping apparatus of claim 7, wherein the first group of modules comprises the i=1 row of the array and the second group of modules comprises the i=2k-1 row of the array.

- 9. The mapping apparatus of claim 5, wherein there are at least $(2k-1)\times 2^{k-1}$ modules and at least $(2k-1)\times 2^{k-1}$ bits, where $p=2^k$ and k>0.
- 10. A process of forming a control bit table for a routing multiplexer that provides p outputs based on a selected permutation of p inputs, the process comprising steps of:
- a) defining the selected permutation having a length n, where $n \ge p$;
- b) identifying first and second groups of vertices each containing alternate vertices of a graph of the selected permutation;
- c) calculating first and second permutations based on respective first and second groups of vertices; and
- d) forming the control bit table based on the first and second permutations and on the vertices of the graph of the selected permutation.
- 11. The process of claim 10, wherein step b) is performed by steps of:
- b1) constructing a graph of the selected permutation having m edges and m vertices arranged in the order of the selected permutation, where n=2m,
- b2) assigning a first color to first alternate edges along the graph and a second color to second alternative edges so that each vertex is connected to

an incoming edge having one color and an outgoing edge having a different color, and

- b2) assigning each vertex the color of one of the incoming and outgoing edges.
- 12. The process of claim 11, wherein each of the vertices has a value, and step c) is performed by steps of:
- c1) assigning the vertices having the first color to a first row and assigning the vertices having the second color to a second row, the vertices in each row being arranged in the order of the selected permutation,
- c2) calculating the first and second permutations based on the values of vertices in the respective first and second rows.
- 13. The process of claim 12, wherein the first permutation comprises values related to one-half the values of the vertices in the first row and the second permutation comprises values related to one-half the values of the vertices in the second row.
- 14. The process of claim 12, wherein step d) is performed by steps of:
- d1) calculating first and second partial control bit tables based on the respective first and second permutations,
 - d2) pairing the vertices in a natural order,

- $\operatorname{d3}$) pairing the vertices in the order of the selected permutation,
- d4) selecting bits of a first bit string based on the color of a selected vertex of each pair of vertices of the natural order,
- d5) selecting bits of a second bit string based on the color of a selected vertex of each pair of vertices of the selected permutation,
- d6) providing the first and second bit strings as the first and last rows, respectively, of the control bit table, and
- d7) concatenating the first and second partial control bit tables as one or more rows of the control bit table between the first and last rows.
- 15. The process of claim 10, wherein each of the vertices has a value, and step c) is performed by steps of:
- c1) assigning the vertices of the first group to a first row and assigning the vertices of the second group to a second row, the vertices in each row being arranged in the order of the selected permutation,
- c2) calculating the first and second permutations based on the values of vertices in the respective first and second rows.
- 16. The process of claim 15, wherein the first permutation comprises values related to one-half the

values of the vertices in the first row and the second permutation comprises values related to one-half the values of the vertices in the second row.

- 17. The process of claim 10, wherein step d) is performed by steps of:
- dl) calculating first and second partial control bit tables based on the respective first and second permutations,
 - d2) pairing the vertices in a natural order,
- d3) pairing the vertices in the order of the selected permutation,
- d4) selecting bits of a first bit string based on the color of a selected vertex of each pair of vertices of the natural order,
- d5) selecting bits of a second bit string based on the color of a selected vertex of each pair of vertices of the selected permutation,
- d6) providing the first and second bit strings as the first and last rows, respectively, of the control bit table, and
- d7) concatenating the first and second partial control bit tables as one or more rows of the control bit table between the first and last rows.
- 18. A process of forming an integrated circuit for mapping memories for parallel turbo decoding employing forming a plurality of control bit tables

in accordance with claim 10, each bit table having at least $(2k-1)\times 2^{k-1}$ bits, the process further including:

- e) storing the control bit tables in a control memory,
- f) forming a multiplexer having a plurality of modules each having first and second inputs, first and second outputs and a control input coupled to the control memory to receive a respective bit from one of the control bit tables, each module being arranged to supply signals at the first and second inputs to the first and second outputs in a direct or transposed order based on a value of the bit at the control input,
- g) coupling an output of each memory to respective ones of the first and second inputs of a first p/2 group of the modules, and
- h) selecting a respective control bit table to supply bits to the control inputs of the modules.
- 19. The process of claim 18, wherein there are at least $(2k-1)\times 2^{k-1}$ modules and at least $(2k-1)\times 2^{k-1}$ bits, where $p=2^k$ and k>0.
- 20. The process of claim 18, wherein the modules are arranged in an array of 2k-1 rows each containing 2^{k-1} modules, and each control bit table contains 2k-1 rows each containing 2^{k-1} bits, where $p=2^k$ and k>0, the memory supplying a j-th bit at an i-th row of a selected control bit table to the

corresponding j-th module of the i-th row of the array.